IMP-HOST INTERFACE FLOW DIAGRAMS

The following flow diagrams were extracted from the logic diagrams provided in Appendix B of BEN Report No. 1822. These diagrams indicate the logical sequence of hardware operations which occur within the IMP-HOST interface. The logic names appearing in the blocks correspond to the logic elements found in Appendix B.
PAD = 1 ?
Y
N

WORD LENGTH = 1 ?
Y
N

INREQST ← 1

DATA HAS BEEN TAKEN ?
Y
N

INREQST ← 0

LAST = 1 ?
Y
N

END OF MESSAGE

PAD = 1 ?
Y
N

CLEAR COUNTER
START OUTPUT

COUNTER ← 1
LSTWD ← 0; BTAVL ← 0

OUT REQST ← 1
CLEAR SHIFT REG.

N
STROBE
DATA WORD
= 1?
Y

LOAD SHIFT REGISTER
OUTREQST ← 0
COUNTER ← 1

N
RENBET
= 1/2?
Y

THERE'S YOUR
HOST BIT ← 1

A
RENBET ← 0?
Y
A

THERE'S YOUR HOST BIT ← 0
STAVL ← 0

WORD LENGTH ← 1

Y

N

LSTWD ← 1

Y

N

PULSE SHIFT REG.
INCREMENT COUNTER

LIBIT ← 0

C

Y

N

LSTWD ← 1

Y

END OF MESSAGE